MLP

Carsem
Your Technology Partner

Micro Leadframe Package

Highlights

QFN and SON near CSP packages.

Highly cost effective solutions

Outstanding thermal-electrical performance

The Carsem MLP advantage

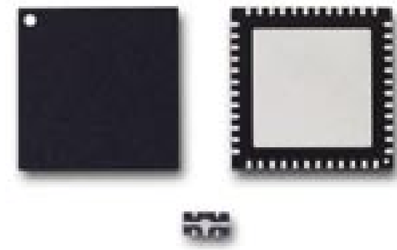
Carsem's MLP (Micro Leadframe Package) is ideal for the demanding applications requiring near chip-size packages with superior thermal-electrical performance. The MLP's are JEDEC compliant QFN (Quad Flat No-Lead) and SON (Small Outline No-lead) plastic packages and are available in QUAD (MLPQ) and Dual (MLPD). Our high-density leadframe design concepts, high through-put singulation methods and innovative technologies allow our MLP to meet the most stringent MSL-1, Pb-free (including NiPdAu terminal finish) and green requirements, while delivering the most cost-effective solutions you need.

To provide even greater utilization of package space and enhanced performance, MLP's are also available using our patented FCOL™ (Flip Chip On Lead) and COL (Chip on Lead) technologies. Optically clear mold compound options are also available. Carsem also offers full turn-key services including RF testing.

Applications:

Excellent choice for many of the new generation devices, especially in the area of RF applications for mobile phones, WiFi, PDA's and Bluetooth™ where size, weight and package performance is required.

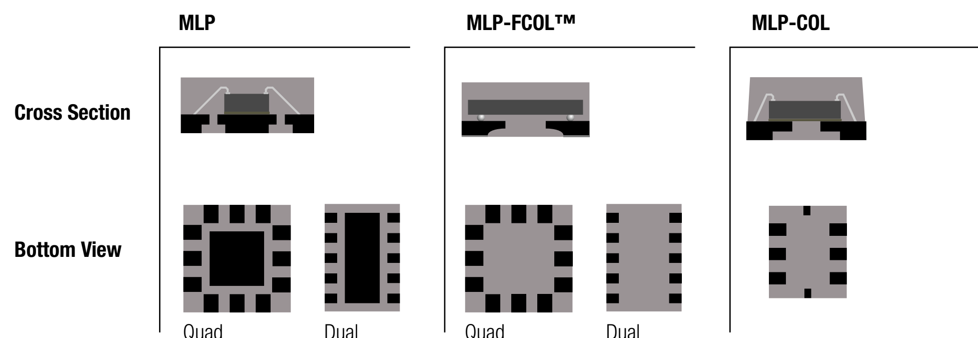
Scale: 3x



2 x 1 mm

Features:

- Small size, weight and height. Typically 1/3 to 1/2 the area of the closest leaded package option.
- Typical 2x to 3x improvement in theta ja and greater than 50% reduction in inductance/capacitance when compared to leaded products with similar I/O count.
- Custom options available in less than 10 days.
- JEDEC MO220 and MO229 compliant.
- Pb-Free (including NiPdAu terminal finish) and Green options available.
- Complete Assembly & Test Solution including RF testing, tape and reel plus drop ship.



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Micro Leadframe Package

MLP Body Size (mm x mm)	Lead Count vs. Lead Pitch (mm)				
	1.27	1.0/0.95	0.8	0.65	0.5*
1.0 x 0.6					2, 3*
2.0 x 2.0				3, 5, 6	6, 8
2.0 x 3.0					8
3.0 x 1.6					6
3.0 x 2.0		5, 6		8	8
3.0 x 3.0		5, 6		8, 8	6, 8, 8, 10, 12, 16
3.0 x 4.0				10	
3.3 x 3.3				8	
3.5 x 3.5					14
4.0 x 3.0					12, 14
4.0 x 3.5					16
4.0 x 4.0			8, 12, 16	10, 12, 16	20, 24
4.0 x 5.0					24
4.5 x 3.5					20, 24
5.0 x 3.0					16
5.0 x 4.0				18	16, 24
5.0 x 5.0	14	12	8	20	16, 28, 32
5.0 x 6.0	8 - SOIC Land Pattern				
5.0 x 7.0					38
5.5 x 3.5					24
6.0 x 5.0					18, 20, 22, 32
6.0 x 6.0				28	36, 40
7.0 x 5.0					38
7.0 x 7.0				32	44, 48
8.0 x 8.0					56
9.0 x 9.0					64

Blue color = Dual version

*Pitches of 0.4mm and below are available for custom designs

MLP Thermal & Electrical Data

Body Size (mm x mm)	Electrical (Typical) L11	C11	Theta Ja (ºC/W)
1 x 2 Dual	0.65	0.07	142
3 x 2 Dual	0.78	0.09	76
3 x 2 COL	0.47	0.08	74
3 x 3 Quad	0.8	0.2	53
5 x 5 Quad	1.1	0.16	37
7 x 7 Quad	1.2	0.17	29
9 x 9 Quad	1.3	0.18	27

L11 - Mutual Inductance (nH)
C11 - Mutual Capacitance (pF)

All Values measured at 2 GHz
COL values assume max die sizes

Theta Ja assumes 4 layer PCB at 0 air flow

MLP Reliability Test Results

Description	Condition	Results
MSL Level 1*	85°C/85%RH for 168 Hrs; 3 x IR @ 260°C	Pass
Auto Clave	121°C/100%RH; 15PSIG; 1008 Hrs	Pass
Temperature Cycle	-65°C/150°C; Air; 1000 Cycles	Pass
Thermal Shock	-55°C/125°C; Liquid; 300 Cycles	Pass
High Temperature Storage	150°C; 1000 Hrs	Pass

* Depending on body size.

This guide is for reference only and Carsem makes no warranty or guarantee of its accuracy. For inquiries or official Carsem documentation, please contact any of our Sales Offices or visit our web site.

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