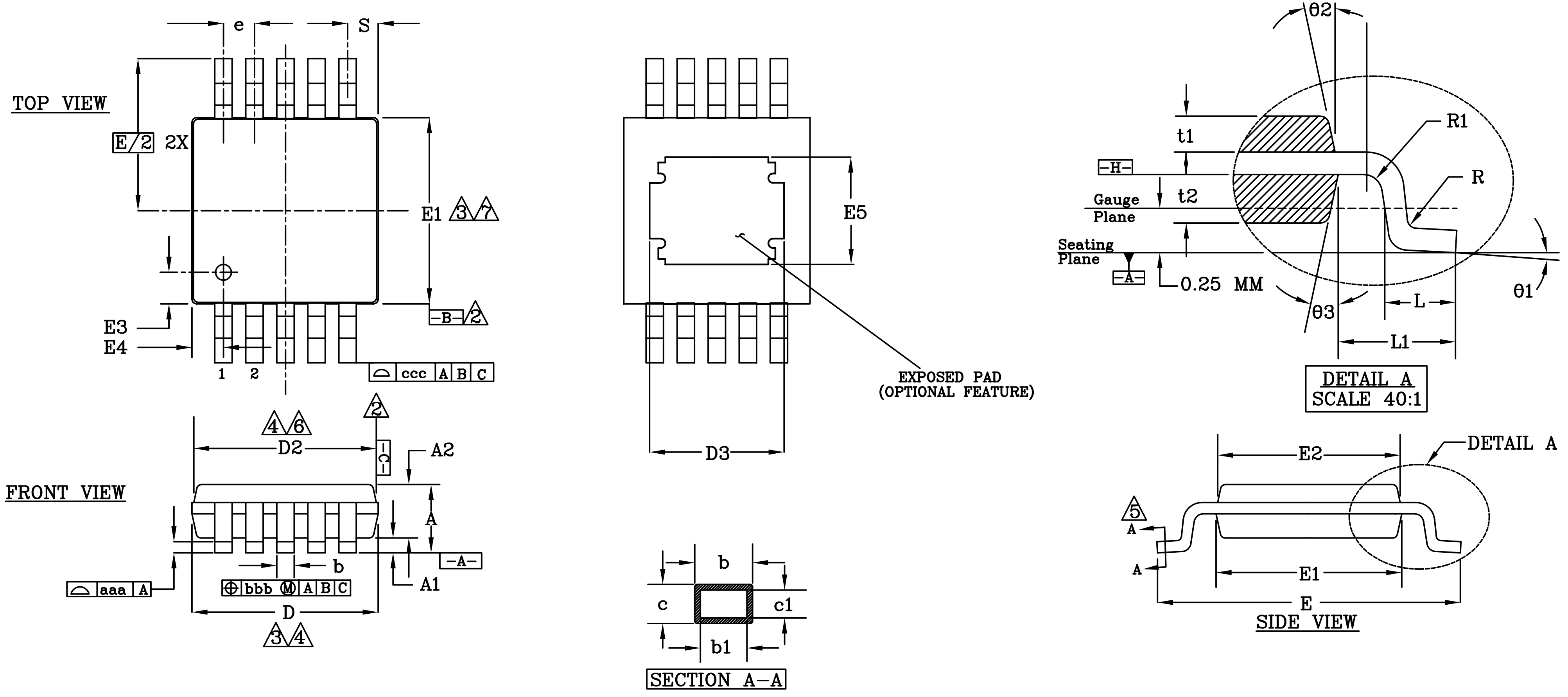

CTC APPROVAL CODE

30070PC4

REV	POS	DESCRIPTION	DATE	BY	APPD
E	—	LEAD WIDTH	2009-JUN-17	SH LOO	—
D	—	EXPOSED PAD OPTION	2006-MAR-17	SH LOO	—
C	—	CHANGED LOGO	2002-APR-03	MK KOK/ KANDA	—

DWG NO PKGS00005

TOLERANCES (INCH/MM)

FRAC ±

ANGLE ±

DECIMALS
X
XX
XXX
XXXX

FINISHING

SYMBOL

REV	E
SCALE	20:1
ORIGINATOR	
TOOLING DEPT MANAGER	
ENGINEERING MANAGER	
QA DEPT MANAGER	
CTC DESIGN DEPT MANAGER	

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TITLE
MINI SOIC 10LD
PACKAGE OUTLINE

REF : CUSTOMER SPECIFICATION

SHEET NO : 1 OF 2

SYMBOL	MINI SOIC 10LD PACKAGE OUTLINE (MILLIMETER)	±TOL
A	1.10	MAX
A1	0.10	±0.05
A2	0.86	±0.08
D	3.00	±0.10
D2	2.95	±0.10
E	4.90	±0.15
E1	3.00	±0.10
E2	2.95	±0.10
E3	0.51	±0.13
E4	0.51	±0.13
R	0.15	$^{+0.15}_{-0.08}$
R1	0.15	$^{+0.15}_{-0.08}$
t1	0.31	±0.08
t2	0.41	±0.08
b	0.23	$^{+0.07}_{-0.06}$
b1	0.20	±0.03
c	0.18	±0.05
c1	0.15	$^{+0.03}_{-0.02}$
θ1	3.0°	±3.0°
θ2	12.0°	±3.0°
θ3	12.0°	±3.0°
L	0.55	±0.15
L1	0.95 BSC	——
aaa	0.10	——
bbb	0.08	——
ccc	0.25	——
e	0.50 BSC	——
S	0.50 BSC	——

SYMBOL	MINI SOIC 10LD – EP1 PACKAGE OUTLINE (MILLIMETER)	±TOL
A	1.10	MAX
A1	0.10	±0.05
A2	0.86	±0.08
D	3.00	±0.10
D2	2.95	±0.10
E	4.90	±0.15
E1	3.00	±0.10
E2	2.95	±0.10
E3	0.51	±0.13
E4	0.51	±0.13
R	0.15	$^{+0.15}_{-0.08}$
R1	0.15	$^{+0.15}_{-0.08}$
t1	0.31	±0.08
t2	0.41	±0.08
b	0.23	$^{+0.07}_{-0.06}$
b1	0.20	±0.03
c	0.18	±0.05
c1	0.15	$^{+0.03}_{-0.02}$
θ1	3.0°	±3.0°
θ2	12.0°	±3.0°
θ3	12.0°	±3.0°
L	0.55	±0.15
L1	0.95 BSC	——
aaa	0.10	——
bbb	0.08	——
ccc	0.25	——
e	0.50 BSC	——
S	0.50 BSC	——
D3	2.18	±0.10
E5	1.73	±0.10

NOTES :

1. ALL DIMENSIONS ARE IN MILLIMETERS (ANGLE IN DEGREES), UNLESS OTHERWISE SPECIFIED.
2. DATUMS $\boxed{-B-}$ AND $\boxed{-C-}$ TO BE DETERMINED AT DATUM PLANE $\boxed{-H-}$.
3. DIMENSIONS "D" AND "E1" ARE TO BE DETERMINED AT DATUM PLANE $\boxed{-H-}$.
4. DIMENSIONS "D2" AND "E2" ARE FOR TOP PACKAGE AND DIMENSIONS "D" AND "E1" ARE FOR BOTTOM PACKAGE.
5. CROSS SECTION A-A TO BE DETERMINED AT 0.13 TO 0.25 MM FROM THE LEADTIP.
6. DIMENSIONS "D" AND "D2" DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS.
7. DIMENSIONS "E1" AND "E2" DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
8. EXPOSED PAD FEATURE IS PRESENT ON VARIATIONS DESIGNATED WITH "-EP"

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REV	POS	DESCRIPTION	DATE	BY	APPD
E	—	LEAD WIDTH	2009-JUN-17	SH LOO	—
D	—	EXPOSED PAD OPTION	2008-MAR-17	SH LOO	—
C	—	CHANGED LOGO	2002-APR-03	MK KOK/ KANDA	—

DWG NO PKGS00005

TOLERANCES (INCH/MM)

FRAC ±

DECIMALS X XX XXX XXXX

ANGLE ±

FINISHING

SYMBOL

REV	E
SCALE	20:1
ORIGINATOR	
TOOLING DEPT MANAGER	
ENGINEERING MANAGER	
QA DEPT MANAGER	
CTC DESIGN DEPT MANAGER	

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TITLE
MINI SOIC 10LD
PACKAGE OUTLINE

REF : CUSTOMER SPECIFICATION

SHEET NO : 2 OF 2